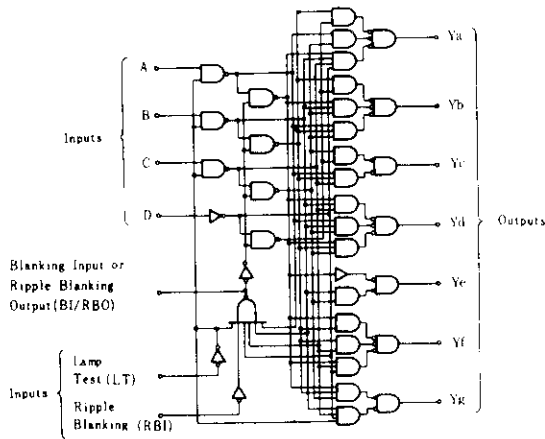


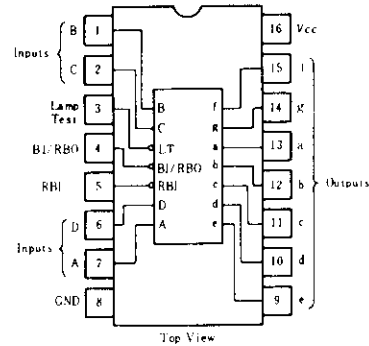
# HD74LS48 • BCD-to-Seven-Segment Decoder/Driver (Internal Pull-up outputs)

The HD74LS48 features active high outputs for driving lamp buffers. This circuit has full ripple blanking input/output controls and a lamp test input. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. It contains an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

## ■ BLOCK DIAGRAM



## ■ PIN ARRANGEMENT



## ■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output current	$I_{OH}$				
	a ~ g	—	—	—100	$\mu A$
Low level output current	$I_{OL}$				
	a ~ g	—	—	6	mA
	BI/RBO	—	—	3.2	mA

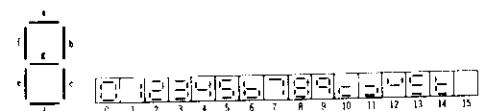
## ■ FUNCTION TABLE

Decimal or Function	Inputs							Outputs							Note
	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	L	L	L	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	L	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	L	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H; high level, L; low level, X; irrelevant

- Notes:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
  2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
  3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When a blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.



## ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	$V_{IH}$		2.0	—	—	V
	$V_{IL}$		—	—	0.8	V
Output voltage	a~g	$V_{OH}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OH} = -100\mu\text{A}$ $I_{OH} = -50\mu\text{A}$	2.4	V
	BI/RBO					
	a~g	$V_{OL}$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OL}=2\text{mA}$ $I_{OL}=6\text{mA}$	—	0.4 0.5
	BI/RBO			$I_{OL}=1.6\text{mA}$ $I_{OL}=3.2\text{mA}$	—	0.4 0.5
						V
Output current **	a~g	$I_O$	$V_{CC}=4.75\text{V}, V_O=0.85\text{V}$	—	—	mA
Input current	except BI/RBO	$I_{IH}$	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	20 $\mu\text{A}$
	BI/RBO	$I_{IL}$	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	—0.4
	BI/RBO	$I_I$	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	—1.2
	except BI/RBO	$I_I$	$V_{CC}=5.25\text{V}, V_I=7\text{V}$	—	—	0.1
Short-circuit output current	BI/RBO	$I_{OS}$	$V_{CC}=5.25\text{V}$	—	—	—2
Supply current ***		$I_{CC}$	$V_{CC}=5.25\text{V}$	—	25	38
Input clamp voltage		$V_{IK}$	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	—1.5

\*  $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

\*\* Input condition as for  $V_{OH}$

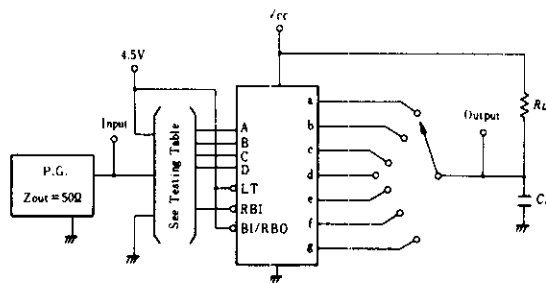
\*\*\*  $I_{CC}$  is measured with all outputs open and all inputs at 4.5V.

## SWITCHING CHARACTERISTICS ( $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$ )

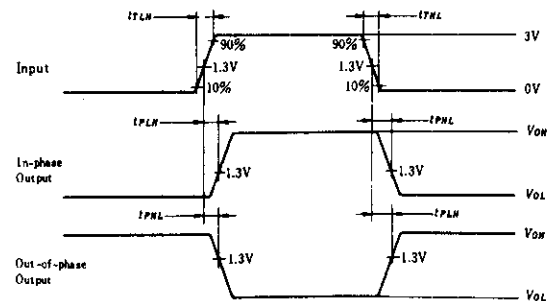
Item	Symbol	Input	Test Conditions	min	typ	max	Unit
Propagation delay time	$t_{PHL}$	A	$C_L=15\text{pF}, R_L=4\text{k}\Omega$	—	—	100	ns
	$t_{PLH}$	A		—	—	100	ns
	$t_{PHL}$	RBI	$C_L=15\text{pF}, R_L=6\text{k}\Omega$	—	—	100	ns
	$t_{PLH}$	RBI		—	—	100	ns

## TESTING METHOD

### 1) Test Circuit

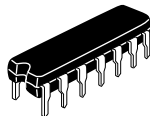
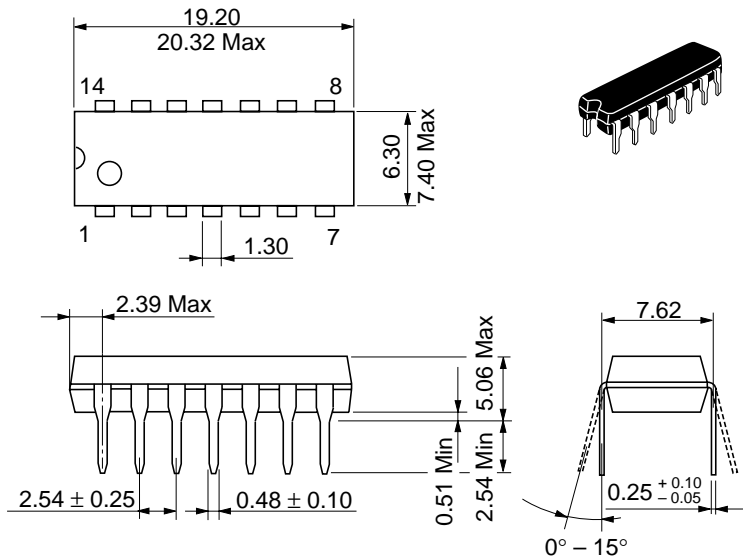


### Waveform

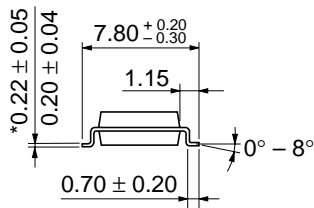
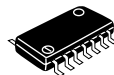
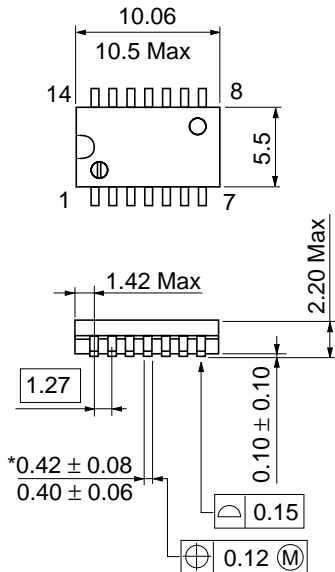


### 2) Testing Table

Item	Inputs					Outputs						
	RBI	D	C	B	A	a	b	c	d	e	f	g
	4.5V	GND	GND	GND	IN	OUT	—	—	OUT	OUT	OUT	—
$t_{PLH}$	4.5V	GND	GND	4.5V	IN	—	—	OUT	—	OUT	—	—
$t_{PHL}$	4.5V	GND	4.5V	4.5V	IN	OUT	OUT	—	OUT	OUT	OUT	OUT
	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT	OUT	—

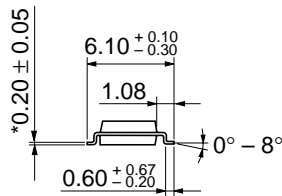
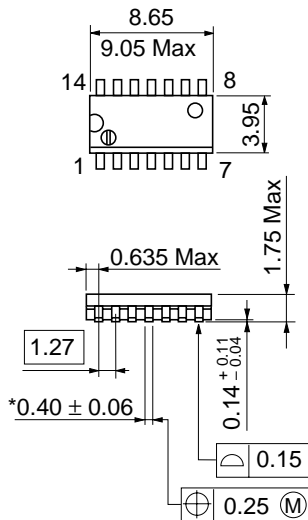


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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